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EXAMINER	
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ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,918	JEDWAB ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- Response to the applicant's amendment dated 1/30/2006
- Amended claims 1-33 have been submitted for examination
- Amended claims 1-33 have been rejected

Response to Arguments

1. Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 25 and 26 is objected to because the word "**means**: should read "**means for**" if the Applicant intended to claim means plus function claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 2, 12, 13, 19, 20, 25-28 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown et al. US patent no. 6360340 (Hereinafter Brown) and further in view of Hughes et al. US patent no. 6,373,758 (Hereinafter Hughes).

4. In regard to claim 1, Brown teaches:

- (Currently amended) A magnetic memory, comprising:
- at least two magnetic memory cells configured to store data, and

(Note: col. 1, line 6 in Brown)

- a control system configured to at least twice obtain parametric values from the magnetic memory cells and generate a corresponding compressed fault map using the parametric values, wherein at least one of the compressed fault maps is compared to a previous one of the compressed fault maps and an indication is provided if there are differences,

(Note: FIG. 2, reference characters (210), (214), (216), (218), (220), (2220 and (224) and col. 6, lines (7-37) in Brown)

However, Brown does not teach:

- said control system further configured to migrate data from said at least two magnetic memory cells to another memory medium in response to the indication.

Hughes in an analogous art teaches self-repairing redundancy allocation for eliminating faulty cells circuit teaches:

- said control system further configured to migrate data from said at least two magnetic memory cells to another memory medium in response to the indication.

(Note: FIG. 5 and col. 10, lines ((49-67) in Hughes)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Hughes with the teaching of Brown to include memory cells repair.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need for efficient use of redundant memory cells.

5. In regard to claim 2, Brown teaches:

- (Original) The magnetic memory of claim 1, wherein each one of The compressed fault maps includes at least one error detection code (col. 3, lines (42-53) in Brown) result which is calculated over the addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic memory cells has a corresponding one of at least two addresses, and wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range.

(Note: col. 5, lines 9-17 in Brown)

6. Claims 12, 19, 25, 27 and 34 are rejected for the same reasons as per claim 1.

7. Claim 13, 20, 26 and 28 are rejected for the same reasons as per claim 2.

8. Claims 3-11,14-18, 21-24, 29-33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown and in further view of Hughes as applied to claim 2 above, and further in view of Yamada et al. US patent no. 6634004 (Hereinafter Yamada).

9. In regard to claim 3 Brown substantially teaches all the limitations in claim 2. However, Brown and further view of Hughes does not teach:

- (Original) The magnetic memory of claim 2, wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

Yamada, in analogous art that teach threshold analysis system capable of deciding all threshold voltages included in memory device teaches:

- (Original) The magnetic memory of claim 2, wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges (Note: Fig. 3, and col. 4, lines (51-67) in Yamada), over the addresses

of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges.

(Note Fig. 3 address ranges in Yamada)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Yamada that comprise of fault maps error diction code with the teaching of Brown and in further view of Hughes.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized the need to efficiently calculate parametric values of memory devices.

10. In regard to claim 4, Yamada teaches:

- (Original) The magnetic memory of claim 1, wherein each one of the compressed fault maps includes at least one error detection code result which is calculated over fault types and corresponding addresses of the magnetic memory cells which have a fault, wherein each one of the magnetic, memory cells has a corresponding one of at least two addresses, wherein the one of the magnetic memory cells has the fault when a corresponding one of the parametric values is not within an expected range, and wherein the corresponding one of the

parametric values is compared to the expected range to infer a corresponding one of the fault types.

(Note: Figures 4 and 5 in Yamada)

11. In regard to claim 5, Yamada teaches:

- (Original) The magnetic memory of claim 41 wherein each one of the compressed fault maps includes at least two error detection code results, wherein each one of the error detection code results is calculated over one of the fault types and the corresponding addresses of all of the magnetic memory cells which have a same one of the fault types.

(Note: Figure 5, any of fail bit information "X" in Yamada)

12. Claims 6, 29 and 32 are rejected for the same reasons as per claim 3.

13. In regard to claim 7, Yamada teaches:

- (Original) The magnetic memory of claim 4, wherein the fault types and the corresponding addresses of the magnetic memory cells are sorted into a numerical order before the error detection code result is calculated.

  Note the sequence of threshold information faults of device under test in FIG.5.

14. In regard to claim 8, Yamada teaches:

- (Original) The magnetic memory of claim 4, wherein the fault types and the corresponding addresses of the magnetic memory cells are sorted

into a numerical order before the error detection code result is calculated.

(Note: col. 7, lines 3-55)in Yamada)

15. In regard to claim 9, Brown teaches:

- (Original) The magnetic memory of claim 4, wherein the error detection code result is calculated using a cyclic redundancy check code.

Note: the RLE "Run Length Encoder" in FIG. 2, reference character (216) in Brown produces fault signature code. The CRC code is a design choice that is obvious over Brown.

16. In regard to claim 10, Yamada teaches:

- (Original) The magnetic memory of claim 1, wherein the previous one of the compressed fault maps is generated using parametric values obtained from the magnetic memory cells the first time that the control system obtains the parametric values from the magnetic memory cells.

(Note: FIG. 4, reference characters (s12), (s14) and (s16) in Yamada)

17. In regard to claim 11, Brown teaches:

- (Original) The magnetic memory of claim 1, wherein the previous compressed fault map is stored in at least one of the magnetic memory cells.

(Note: FIG. 1, reference character (126) in Brown)

18. Claims 15, 22, 30, and 33 are rejected for the same reasons as per claim 4.

19. In regard to claim 24, Hughes teaches:

- (Currently amended) The storage system of claim 22, wherein each one of the error detection code results is calculated for a corresponding one of at least two address ranges, over the fault types and the corresponding addresses of the magnetic memory cells which have the fault and are within a same one of the address ranges, wherein each one of the addresses is within only one of the address ranges, and wherein the control system migrates data by transferring, when the indication is provided, the data from at least one of the address ranges wherein at least one of the magnetic memory cells has fault, to at least one of the address ranges where none of the magnetic memory cells have the fault.

(Note: FIG. 9, reference character (801) in Hughes)

20. Claims 16, 23 and 31 are rejected for the same reasons as per claim 5.

21. Claims 14, 17 and 21are rejected for the same reasons as per claim 3.

22. Claim 18 is rejected for the same reasons as per claim 11.

23. Claim 35 is rejected for the same reasons as per claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax

phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk,

Examiner

ART UNIT 2112/

2/8/08

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